ABSTRACT

An innovative routing method for an integrated circuit design layout. The layout can include design netlists and library cells. A multiple-level global routing can generate topological wire for each net. An area oriented graph-based detail routing on the design can be performed. A post route optimization after the detail routing can be performed to further improve the routing quality. Some methods can be single threaded all or some of the time, and/or multi-threaded some or all of the time.